

REMARKS / DISCUSSION OF ISSUES

In view of the amendments above and the remarks to follow, reconsideration and allowance of this application are respectfully requested.

Status of Claims

Claims 1-17 remain in this application. Claims 1, 10, 14 and 17 have been amended.

Allowable Subject Matter

Applicant wishes to thank the Examiner for indicating that Claims 10 and 14 are allowable and that claims 11-12 and 15-16 are allowable, since they depend on claim 10 and 14, respectively.

35 U.S.C. §112, second paragraph

Claims 1 and 17 were rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The rejection of claims 1 and 17 is understood to be based on the premise that applicant failed to point out supporting detail of the amended limitation “the timing of the end of the pulse corresponding to the timing of an interrupt by the means of interrupting”. Applicant has amended claims 1 and 17 in a manner which is believed to overcome the rejection. In particular, claims 1 and 17 have been amended to unambiguously recite that a drive voltage is generated by the shift register and logic arrangement for the interrupting means. The drive voltage includes a long emission time pulse having a variable duration where the end of the long emission time pulse corresponds to the timing of an interrupt signal generated by the interrupting means.

Claims 1 and 17 recite in relevant part -

wherein the row driver circuitry comprises a shift register arrangement and logic arrangement for generating the drive voltage for the interrupting means, the drive voltage for the interrupting means including a long emission time pulse for controlling the output of the display element, the long emission time pulse having a duration which can be varied up to substantially the full field period less the address period, and wherein the timing of the end of the long emission time

pulse corresponds to the timing of the direct interrupt signal generated by the interrupting means for controlling the display element illumination time,

Applicant respectfully submits that the amended claim recitation is intended to more clearly recite that a drive voltage is generated as input to the interrupting means. The drive voltage includes a pulse having a variable duration. The end of the variable duration pulse corresponds to the timing of the interrupt signal generated by the interrupting means. In other words, the end of the variable duration pulse corresponds to the point in time for controlling the display element illumination time.

Claim Rejections under 35 USC 102

In the Office Action, Claims 1-9, 13 and 17 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,583,775 (“Sekiya”). Applicants respectfully traverse the rejections.

Claims 1-9, 13 and 17 are allowable

In Applicant’s previous response, it was argued that Sekiya is distinguishable from the present invention in that Sekiya teaches an indirect current interruption method while the present invention teaches a direct current interruption method. In the previous Office Action, mail date March 17, 2010, it was suggested by the Office that the transistor TFT3 of Sekiya, as shown in Fig. 1, teaches means for interrupting the drive of current through the display element. In response, Applicants argued that Sekiya is distinguishable from the Applicant’s invention in that the means for interrupting the drive current as taught in Sekiya is an **indirect means of drive current interruption**. In support, it was argued that the indirect means is embodied in a data storage capacitor that must discharge TFT3 to indirectly cause transistor TFT2 to stop conducting. In contrast to the current interruption method of Sekiya, the current is interrupted directly in accordance with the method of the invention. This is achieved by inserting a TFT (28), see Fig. 3, directly into the current path of the display element and switching TFT (2) off to control the display time. As previously argued, the method of Sekiya will not work for direct current interruption. As correctly noted by the Office in the instant action, while the Applicant’s arguments were persuasive, they were not

recited as a distinguishing feature in the rejected claims. See, *Response to Arguments*, at page 8 of the instant Office Action.

Accordingly, Independent claim 1 has been amended in part to incorporate the aforementioned distinguishing feature. It is therefore respectfully submitted that claim 1 now recites limitations and/or features which are not disclosed by Sekiya. Accordingly, the cited portions of Sekiya do not anticipate claim 1, because the cited portions of Sekiya fail to disclose every element of claim 1. For example, the cited portions of Sekiya fail to disclose or suggest,

means for directly interrupting the drive of current through the display element via a direct interrupt signal. said interrupting means being provided in series with the electroluminescent display element; and

wherein the row driver circuitry comprises a shift register arrangement and logic arrangement for generating the drive voltage for the interrupting means, the drive voltage for the interrupting means including a long emission time pulse for controlling the output of the display element, the long emission time pulse having a duration which can be varied up to substantially the full field period less the address period, and wherein the timing of the end of the long emission time pulse corresponds to the timing of **the direct interrupt signal generated by the interrupting means for controlling the display element illumination time**,

In further contrast to Sekiya, Applicants respectfully submit that Sekiya does not teach or suggest, “a long emission time pulse for controlling the output of the display element.” Instead, Sekiya is simply controlled with a pulse that is a delayed version of the row address pulse, where the delayed version of the row address pulse is synchronized to the vertical clock signal so that the emission of light is successively stopped in a unit of a scanning line. See, Sekiya, Col. 12, as repeated below.

Sekiya discloses at Col 12 -

FIG. 3 illustrates operation of the image display apparatus described above with reference to FIGS. 1 and 2. Referring to FIG. 3, a vertical start pulse VSP1 is first inputted to the scanning line drive circuit 21 and the delay circuit 24. After the scanning line drive circuit 21 receives the vertical start pulse VSP1 inputted thereto, it successively selects the scanning lines X1, X2, . . . , XN in synchronism with the vertical clock signal VCK so that brightness information is successively written into the pixels PXL in a unit of a scanning line. Each of the pixels PXL starts emission of light with a level of intensity corresponding to the brightness information written therein. The vertical start pulse VSP1 is delayed by the delay circuit 24 and inputted as the vertical start pulse VSP2 to the stopping control line drive circuit 23. **After the stopping control line drive circuit 23 receives the vertical start pulse VSP2, it successively selects the stopping control lines Z1, Z2, . . . , ZN in synchronism with the vertical clock signal VCK so that the emission of light is successively stopped in a unit of a scanning line.**

As described above, Sekiya teaches that the vertical start pulse is input to the scanning line drive circuit 21 and the delay circuit 24. After the scanning line drive circuit 21 receives the vertical start pulse VSP1 inputted thereto, it successively selects the scanning lines X1, X2, . . . , XN in synchronism with the vertical clock signal VCK so that brightness information is successively written into the pixels PXL in a unit of a scanning line. Each of the pixels PXL starts emission of light with a level of intensity corresponding to the brightness information written therein. The vertical start pulse VSP1 is delayed by the delay circuit 24 and inputted as the vertical start pulse VSP2 to the stopping control line drive circuit 23. After the stopping control line drive circuit 23 receives the vertical start pulse VSP2, it successively selects the stopping control lines Z1, Z2, . . . , ZN **in synchronism with the vertical clock signal VCK so that the emission of light is successively stopped in a unit of a scanning line.**

It is therefore shown that the interrupt device of Sekiya is simply controlled with a pulse that is a delayed version of the row address pulse, where the delayed version of the row address pulse is synchronized to the vertical clock signal so that the emission of light is successively stopped in a unit of a scanning line. In contrast to Sekiya, the invention discloses an interrupt device that **cannot** simply be controlled with a pulse which is a delayed version of the row address pulse and **is not** in synchronism with a vertical clock signal so that the emission of light is successively stopped in a unit of a scanning line. Instead, **a long**

emission time pulse is required, with the timing of the end of the pulse corresponding to independently derived **interrupt timing**, and not the vertical clock signal, as taught in Sekiya.

It should be appreciated that such a long emission time pulse having an end timing corresponding to the interrupt timing is different from a simple delayed version of a row address pulse, as taught in Sekiya. In accordance with the operation of Applicant's invention, two shift registers A and B are used with the row drivers. In one embodiment, a single pulse is propagated down the first shift register a, which selects the row to be addressed, while a second single-pulse is propagated down the second shift register B. The time difference between them is used to generate the long emission-time pulse, which controls the output of the display element. Other embodiments may generate the long emission-time pulse in other ways, as described in Applicant's specification. The long emission time pulse is a variable duration emission signal that is derived from the time difference there-between, as stated above, and is **not** synchronized to the vertical clock signal. A row control signal A3r is derived from the long emission time pulse as input to the interrupting transistor 28 (see Fig. 3) having an on pulse of variable duration.

A further distinguishing feature is that the "on" pulse duration is typically a number of row address period durations, and thus varies with the frame time and **not** within the line time. It is respectfully submitted that Sekiya does not teach or suggest a derived signal synchronized to the frame time. Instead, the light emitting elements included in the pixels are extinguished collectively in a unit of a scanning line before brightness information of a next scanning line cycle (frame) is newly written into the pixels.

According to Sekiya, the image display apparatus may be constructed such that it further comprises a scanning line drive circuit to which a vertical clock signal for successively selecting the scanning lines and a control means includes a control circuit for receiving another vertical clock signal obtained by delaying the vertical clock signal by a predetermined period to select the scanning lines or control lines provided in parallel to the scanning lines, and the scanning lines are successively selected in synchronism with the vertical clock signal by the scanning line drive circuit to light the pixels, the pixels which have been lit being extinguished over the scanning line or the control lines within the period of one scanning

cycle in synchronism with the delayed vertical clock signal by the control circuit. In this instance, the image display apparatus may be constructed further such that it further comprises a data line drive circuit for providing the brightness information to the data lines, and that each of outputs of the scanning line drive circuit is connected to an input terminal of a logical OR circuit having an output terminal connected to one of the scanning lines while each of outputs of the control circuits is connected an input terminal of a logical AND circuit connected to the other input terminal of the logical OR circuit, and the vertical clock signal is inputted to the other input terminal of the logical AND circuit. after brightness information is written into the pixels in a unit of a scanning line, **the light emitting elements included in the pixels are extinguished collectively in a unit of a scanning line before brightness information of a next scanning line cycle (frame) is newly written into the pixels.** Or in other words, after brightness information is written into each pixel and the pixel begins to emit light, the emission of light can be stopped before writing of a next frame is performed. Consequently, the time from lighting to extinction of the light emitting elements after brightness information is written into the pixels can be adjusted. In other words, the ratio (duty) of the time of light emission within one scanning cycle or one frame can be adjusted. The adjustment of the time of light emission (duty) corresponds to adjustment of the peak current of each light emitting element. Therefore, by adjusting the duty, the display brightness, that is, the display brightness average in time, can be adjusted simply and freely. What is more significant is that the peak current can be increased by setting the duty appropriately. For example, if the duty is reduced to $1/10$, then an equal brightness value is obtained even if the peak current is increased to 10 times. If the peak current is increased to 10 times, then the channel length of a thin film transistor included in each pixel can be reduced to $1/10$. In this manner, by suitably selecting the duty, the degree of freedom in designing a thin film transistor included in each pixel increases, and this allows practical designing. Further, since the duty can be set freely, a degree of freedom is provided in that the amount of current to flow to each light emitting element upon light emission is set suitably while the display brightness average in time is kept equal. Consequently, a degree of freedom in designing of an active element for controlling the amount of current to flow to the light emitting element is produced. As a result, it becomes possible to design an image display apparatus which can provide an image of a higher degree of picture quality or another image

display apparatus of a smaller pixel size.

Hence claim 1 is allowable and claims 2-9 and 13 are allowable, at least by virtue of their respective dependence from claim 1.

Independent Claim 17 recites similar subject matter as Claim 1 and therefore contains the limitations of Claim 1. Hence, for at least the same reasons given for Claim 1, Claim 17 is believed to contain patentable subject matter.

Conclusion

In addition, Applicant denies any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicant reserves the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to credit any overpayment or charge any fee (except the issue fee) including fees for any required extension of time, to Account No. 14-1270.

Respectfully submitted,

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